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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,677	02/01/2002	Robert J. Devins	BUR920010098	3095

30449 7590 02/26/2007

SCHMEISER, OLSEN & WATTS
22 CENTURY HILL DRIVE
SUITE 302
LATHAM, NY 12110

EXAMINER	
ALHIJA, SAIF A	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/683,677	DEVINS ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,5,7,14,16,17,19,21 and 31-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5,7,14,16,17,19,21 and 31-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2, 3, 5, 7, 14, 16, 17, 19, 21, and 31-36 have been presented for examination.

Claims 1, 4, 6, 8-13, 15, 18, 20, and 22-30 have been cancelled.

Claims 31-36 are newly added.

Response to Arguments

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15 December 2006 has been entered.

i) Applicant's arguments filed 15 December 2006 have been fully considered and are moot in view of the new grounds of rejection presented below.

Claim Objections

3. **Claim 21 is objected** to because of the following informalities:

Claim 21 recites "a simulated serial cores." The claim should recite "a simulated serial core."

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02. A process that consists solely of the manipulation of an abstract idea is not concrete or

tangibles. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed.Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

4. **Claims 2, 3, 5, 7, 14, 16, 17, 19, 21, and 31-36 are rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

i) Claims 31 and 32 recite a program storage device/compute readable memory unit as well as method steps. This appears to be a mixing of statutory classes which renders the claims non-statutory since the specific statutory category of the claims cannot be ascertained.

ii) Claims 14, 31 and 32 recite a method, system/computer readable memory, and program storage device/method that are all code. This is reinforced in Page 10 of Applicants Arguments dated 15 December 2006 in which Applicant states:

> The term "simulated" as used in the claims was discussed in the context of Applicants invention being completely implemented in software (except for the computer running the software) as opposed to the prior art having a hardware model with memory devices simulating buses.

It should be noted that code (i.e., a computer software program) does not do anything per se. Instead, it is the code stored on a computer that, *when executed*, instructs the computer to perform various functions. The following claim is a generic example of a proper computer program product claim;

A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

> Function A
> Function B
> Function C, etc...

All claims dependent upon rejected base claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 2, 3, 5, 7, 16, 17, 19, 21, and 31-32 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i) Claims 31 and 32 recite "programmably connectable" which renders the claim vague and indefinite. The term programmably is defined to be "capable of being processed with computer instructions." It is unclear if this term refers to a user providing a program, an automated program, a program that is dynamic and either automated or supplied by a user, etc. The way in which the switch is "programmably connectable" to the I/O driver models is unclear. A predefined program, a user provided program that is dynamic, or an automated dynamic program would all require differing structural elements and therefore since the claim does not expand on the term or provide necessary structural elements to clearly define the term, the term renders the claim vague and indefinite. Further, the phrase "programmably connectable" is used in conjunction with a simulated switch in the claims. However, the claims do not further expand on the way the driver models are connected to the switch. The claim recites simulated I/O buses yet it is unclear if the simulated buses refers directly to the "programmably connectable" portion of the claims or are distinctly stated. Additional clarification is requested.

Appropriate correction is required.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claim(s) 2, 3, 5, 7, 14, 16, 17, 19, and 31-36 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **Dearth et al. "Virtual Bus For Distributed Hardware Simulation", U.S. Patent No. 5,881,267,** hereafter referred to as **Dearth.**

Regarding Claim 2:

The reference discloses The computer system of claim 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective I/O driver models. **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit) (Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts) (Dearth. Column 1, Lines 59-65, for registers. Column 6, Lines 33-67 which discloses register data and transaction.)**

Regarding Claim 3:

The reference discloses The system of claim 31, wherein said simulated external memory mapped test device further includes a simulated address register. **(Dearth. Column 1, Lines 59-65, for registers. Column 6, Lines 33-67 which discloses register data and transaction.)**

Regarding Claim 5:

The reference discloses The system of claim 2, wherein each said simulated external memory mapped test device module further includes a simulated address register. **(Dearth. Column 1, Lines 59-65, for registers. Column 6, Lines 33-67 which discloses register data and transaction.)**

Regarding Claim 7:

The reference discloses The system of claim 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective I/O driver model of said one or more I/O driver models and further including the method steps of :

loading code representing an additional simulated external memory mapped test device module into said memory unit; **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit)**

said loading of said test case connecting one or more additional I/O driver models to said additional simulated external memory mapped test device by additional simulated I/O buses; and **(Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

said loading of said test case connecting each additional I/O driver model to a respective additional simulated I/O core by said simulated system bus, each additional simulated I/O core comprising said model of integrated circuit design. **(Dearth. Column 6, Lines 33-67 which discloses test data and simulation of a simulated circuit.)**

Regarding Claim 14:

The reference discloses A method for verifying an integrated circuit design comprising:

providing a simulated I/O controller connected to one or more simulated I/O cores, said simulated I/O cores part of said integrated circuit design; **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit. Circuit parts represent cores, for example)**

providing a simulated external memory mapped test device having a simulated switch for selectively connecting one or more of said simulated I/O cores to corresponding simulated I/O driver models; **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

providing a simulated bus for transferring simulated, signals between said simulated I/O controller and said simulated switch; **(Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

providing a test operating system for allocating I/O pins of said simulated I/O controller and for connecting said simulated switch to said external memory mapped device and to simulated I/O driver models; **(Dearth. Column 6, Lines 33-67 which discloses test data and simulation of a simulated circuit)** and

simulating said integrated circuit design by running a test case on said test operating system. **(Dearth. Column 6, Lines 33-67 which discloses test data and simulation of a simulated circuit)**

Regarding Claim 16:

The reference discloses The program storage device of claim 32, said method steps further including:

distributing said simulated external memory mapped test device and said simulated switch among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory modules containing a portion of said simulated switch and connected to one of said simulated I/O driver models. **(Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

Regarding Claim 17:

The reference discloses The program storage device of claim 32, said method steps further including:

providing said simulated external memory mapped test device with a simulated address register; and setting said simulated switch and controlling said simulated I/O driver using address information programmed into said simulated address register. **(Dearth. Column 1, Lines 59-65, for registers. Column 6, Lines 33-67 which discloses register data and transaction.)**

Regarding Claim 19:

The reference discloses The program storage device of claim 16, said method steps further including:

providing each simulated external memory mapped test device with a simulated address register; **(Dearth. Column 1, Lines 59-65, for registers. Column 6, Lines 33-67 which discloses register data and transaction.) (Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)** and

setting each portion of said simulated switch and controlling each simulated I/O driver using address information programmed into said simulated address register. **(Dearth. Column 1, Lines 59-65, for registers. Column 6, Lines 33-67 which discloses register data and transaction.) (Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

Regarding Claim 31:

The reference discloses A computer system comprising a processor and a computer-readable memory unit coupled to communicate with said processor, said memory unit containing instructions that when executed by the processor implement a method for verifying an integrated circuit design, said method comprising the computer implemented steps of:

loading code representing said integrated circuit design into said memory unit, said integrated circuit design including simulated I/O cores, a simulated external memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus; **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit. Circuit parts represent cores, for example)**

loading code representing an external memory model, a simulated external memory mapped test device and one or more I/O driver models into said memory unit, said simulated external memory mapped test device including a simulated switch programmably connectable to said one or more I/O driver models, to said simulated I/O controller and to said external memory model, said I/O driver models connected to corresponding said simulated I/O cores by corresponding simulated I/O buses; **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts) (Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

loading a test case comprising a list of computer-executable instructions on said simulated processor, said loading of said test case allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said simulated external memory mapped test device to said simulated I/O controller and to said one or more of said simulated I/O cores; **(Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

executing test stimuli of said test case on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case; **(Dearth. Column 6, Lines 33-67 which discloses test data and simulation of a simulated circuit)** and

outputting said data representing a response of said computer simulation model of said integrated circuit design to said test case. **(Dearth. Column 6, Lines 33-67 which discloses test data and simulation of a simulated circuit)**

Regarding Claim 32:

The reference discloses A program storage device readable by machine, tangibly embodying a program of instructions executable by machine to perform method steps a method for verifying an integrated circuit design, said method steps comprising:

generating a model of said integrated circuit design, said integrated circuit design including simulated I/O cores, a simulated external memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus; **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit. Circuit parts represent cores, for example)**

generating an external memory model, a simulated external memory mapped test device and one or more I/O driver models, said simulated external memory mapped test device including a simulated switch programmably connectable to said one or more I/O driver models, to said simulated I/O controller and to said external memory model, said I/O driver models connected to corresponding said simulated I/O cores by corresponding simulated I/O buses; **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts) (Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

loading a test case comprising a list of computer-executable instructions on said simulated processor, said loading of said test case allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said simulated external memory

mapped test device to said simulated I/O controller and to said one or more of said simulated I/O cores; **(Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts) (Dearth. Column 6, Lines 33-67 which discloses test data and simulation of a simulated circuit)**and

executing test stimuli of said test case on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case. **(Dearth. Column 6, Lines 33-67 which discloses test data and simulation of a simulated circuit)**

Regarding Claim 33:

The reference discloses The method of claim 14, further including:

distributing said simulated external memory mapped test device and said simulated switch among a plurality of simulated external memory mapped test device modules, each simulated external memory mapped test device module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to one of said plurality of simulated external memory mapped test device modules I/O driver models: **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit) (Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)** and

providing an additional simulated external memory mapped test device module directly connected to one or more additional plurality of simulated external memory mapped test device modules I/O driver models, each additional plurality of simulated external memory mapped test device modules I/O driver model of said additional plurality of simulated external memory mapped test device modules directly connected to an additional simulated I/O core, each additional simulated I/O core part of said integrated circuit design. **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a**

simulated circuit) (Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)

Regarding Claim 34:

The reference discloses The method of claim 14, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to respective I/O driver models. **(Dearth. Column 6, Lines 33-67 which discloses I/O and simulation of a simulated circuit) (Dearth. Column 4, Lines 31-47 which discloses multiple VBS' connecting different circuit parts)**

Regarding Claim 35:

The reference discloses The method of claim 14, wherein said simulated external memory mapped test device further includes a simulated address register. **(Dearth. Column 1, Lines 59-65, for registers. Column 6, Lines 33-67 which discloses register data and transaction.)**

Regarding Claim 36:

The reference discloses The method of claim 14, wherein each said simulated external memory mapped test device module further includes a simulated address register. **(Dearth. Column 1, Lines 59-65, for registers. Column 6, Lines 33-67 which discloses register data and transaction.)**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. **Claim(s) 21 is** rejected under 35 U.S.C. 103(a) as being unpatentable over **Dearth** in view of **Dutta et al. "Viper"**, hereafter referred to as **Dutta .**

Regarding Claim 21:

Dearth does not explicitly disclose The computer system of claim 31, wherein said one or more simulated I/O cores includes a simulated universal asynchronous receiver transmitter core, a simulated serial cores, a simulated general purpose I/O core, a direct memory access core or combinations thereof.

Dutta discloses multiple types of cores. **(Dutta. Page 21, Paragraph 3. Page 22. Figure 1)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the cores discussed in **Dutta** for the simulation system of **Dearth** in order to allow for proper verification of all popular input output formats.

Further, the cores discussed are an intended use of claim 21. As per MPEP Section 2106, Section II.C, *"Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation."* The limitations of claim 21 are merely a type of core being verified by the system described in claim 31 and do not reflect a further limitation in the structure and therefore the scope of the claim.

8. **Claim(s)) 2, 3, 5, 7, 14, 16, 17, 19, and 31-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Evans et al. "Apparatus and Method for Verifying a Multi-Component Electronic Design", U.S. Patent No. 6,279,146,** hereafter referred to as **Evans.**

Regarding Claim 2:

Evans discloses The computer system of claim 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective I/O driver models. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.) (Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus line and has a**

control block controlling the switchable communicative circuitry.") (Evans. Figure 5, element 146. Column 11, Line 14 which states "virtual buses.")

Evans does not explicitly disclose simulated components, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 3:

Evans discloses The system of claim 31, wherein said simulated external memory mapped test device further includes a simulated address register. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.)**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 5:

Evans discloses The system of claim 2, wherein each said simulated external memory mapped test device module further includes a simulated address register. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.)**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 7:

Evans discloses The system of claim 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective I/O driver model of said one or more I/O driver models and further including the method steps of :

loading code representing an additional simulated external memory mapped test device module into said memory unit; **(Evans. Figures 2, 5, and 6. Column 2, Lines 13-37, specifically 30-32 which states, "Alternatively, the debug package could be used without the hardware components. This will, of course, not find problems that occur in the interaction of the software and the hardware. The early use of such a debug package would be tremendously beneficial to software developers in their efforts to debug software prior to the time when an entire system has been constructed. " Column 3, Lines 49-62, specifically "Virtual Components" which are loadable files and therefore software.)**

said loading of said test case connecting one or more additional I/O driver models to said additional simulated external memory mapped test device by additional simulated I/O buses; **(Evans. Column 2, Lines 4-6 which states "Unfortunately, software verification requires an order of magnitude more simulation patterns to verify than does hardware verification.") (Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus line and has a control block controlling the switchable communicative circuitry.")**

and

said loading of said test case connecting each additional I/O driver model to a respective additional simulated I/O core by said simulated system bus, each additional simulated I/O core comprising said model of integrated circuit design. **(Evans. Column 2, Lines 4-6 which states "Unfortunately, software verification requires an order of magnitude more simulation patterns to verify than does hardware verification.") (Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus line and has a control block controlling the switchable communicative circuitry.")**

Evans does not explicitly disclose that every component is a simulated component,, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 14:

Evans discloses A method for verifying an integrated circuit design comprising:

providing a simulated I/O controller connected to one or more simulated I/O cores, said simulated I/O cores part of said integrated circuit design; **(Evans. Figures 2, 5, and 6. Column 2, Lines 13-37, specifically 30-32 which states, "Alternatively, the debug package could be used without the hardware components. This will, of course, not find problems that occur in the interaction of the software and the hardware. The early use of such a debug package would be tremendously beneficial to software developers in their efforts to debug software prior to the time when an entire system has been constructed. " Column 3, Lines 49-62, specifically "Virtual Components" which are loadable files and therefore software.)**

providing a simulated external memory mapped test device having a simulated switch for selectively connecting one or more of said simulated I/O cores to corresponding simulated I/O driver

models; **(Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus line and has a control block controlling the switchable communicative circuitry.")**

providing a simulated bus for transferring simulated, signals between said simulated I/O controller and said simulated switch; **(Evans. Figure 5, element 146. Column 11, Line 14 which states "virtual buses.")**

providing a test operating system for allocating I/O pins of said simulated I/O controller and for connecting said simulated switch to said external memory mapped device and to simulated I/O driver models; **(Evans. Figure 2, Element 114)** and

simulating said integrated circuit design by running a test case on said test operating system. **(Evans. Column 2, Lines 4-6 which states "Unfortunately, software verification requires an order of magnitude more simulation patterns to verify than does hardware verification.")**

Evans does not explicitly disclose that every component is a simulated component representing the I/O controller, I/O cores, EMMTD, switch, I/O driver models, and bus.

However Evans teaches that software verification is an order of magnitude slower than hardware verification, therefore, the process of verification is improved by implementing certain components in hardware. This not only teaches the use of software verification for components and packages but also that the implementation discussed in **Evans** is a step forward in the art by increasing the speed and therefore decreasing the time of verification. The implementation discussed in Evans reads on the implementation discussed in the claims of the instant application. **(Evans. Column 1, Lines 31-39 for example)**

It would have been obvious to one of ordinary skill in the art to implement the verification in **Evans** by utilizing software instead of hardware in order to debug software prior to construction of the system being verified. **(Evans. Column 2, Lines 30-32)**

Regarding Claim 16:

Evans discloses The program storage device of claim 32, said method steps further including:

distributing said simulated external memory mapped test device and said simulated switch among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory modules containing a portion of said simulated switch and connected to one of said simulated I/O driver models. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.) (Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus line and has a control block controlling the switchable communicative circuitry.") (Evans. Figure 5, element 146. Column 11, Line 14 which states "virtual buses.")**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 17:

Evans discloses The program storage device of claim 32, said method steps further including:

providing said simulated external memory mapped test device with a simulated address register; and setting said simulated switch and controlling said simulated I/O driver using address information

programmed into said simulated address register. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.)**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 19:

Evans discloses The program storage device of claim 16, said method steps further including:

providing each simulated external memory mapped test device with a simulated address register; and

setting each portion of said simulated switch and controlling each simulated I/O driver using address information programmed into said simulated address register. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.)**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 31:

Evans discloses A computer system comprising a processor and a computer-readable memory unit coupled to communicate with said processor, said memory unit containing instructions that when

executed by the processor implement a method for verifying an integrated circuit design, said method comprising the computer implemented steps of:

loading code representing said integrated circuit design into said memory unit, said integrated circuit design including simulated I/O cores, a simulated external memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus; **(Evans. Figures 2, 5, and 6. Column 2, Lines 13-37, specifically 30-32 which states, "Alternatively, the debug package could be used without the hardware components. This will, of course, not find problems that occur in the interaction of the software and the hardware. The early use of such a debug package would be tremendously beneficial to software developers in their efforts to debug software prior to the time when an entire system has been constructed. " Column 3, Lines 49-62, specifically "Virtual Components" which are loadable files and therefore software.)**

loading code representing an external memory model, a simulated external memory mapped test device and one or more I/O driver models into said memory unit, said simulated external memory mapped test device including a simulated switch programmably connectable to said one or more I/O driver models, to said simulated I/O controller and to said external memory model, said I/O driver models connected to corresponding said simulated I/O cores by corresponding simulated I/O buses; **(Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus line and has a control block controlling the switchable communicative circuitry.") (Evans. Figure 5, element 146. Column 11, Line 14 which states "virtual buses.")**

loading a test case comprising a list of computer-executable instructions on said simulated processor, said loading of said test case allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said simulated external memory

mapped test device to said simulated I/O controller and to said one or more of said simulated I/O cores; **(Evans. Figure 2, Element 114)**

executing test stimuli of said test case on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case; **(Evans. Figure 2, Element 114) (Evans. Column 2, Lines 4-6 which states "Unfortunately, software verification requires an order of magnitude more simulation patterns to verify than does hardware verification.")** and

outputting said data representing a response of said computer simulation model of said integrated circuit design to said test case. **(Evans. Figure 2, Element 114) . (Evans. Column 2, Lines 4-6 which states "Unfortunately, software verification requires an order of magnitude more simulation patterns to verify than does hardware verification.")**

Evans does not explicitly disclose that every component is a simulated component representing the I/O controller, I/O cores, EMMTD, switch, I/O driver models, and bus.

However Evans teaches that software verification is an order of magnitude slower than hardware verification, therefore, the process of verification is improved by implementing certain components in hardware. This not only teaches the use of software verification for components and packages but also that the implementation discussed in **Evans** is a step forward in the art by increasing the speed and therefore decreasing the time of verification. The implementation discussed in Evans reads on the implementation discussed in the claims of the instant application. **(Evans. Column 1, Lines 31-39 for example)**

It would have been obvious to one of ordinary skill in the art to implement the verification in **Evans** by utilizing software instead of hardware in order to debug

software prior to construction of the system being verified. **(Evans. Column 2, Lines 30-32)**

Regarding Claim 32:

Evans discloses A program storage device readable by machine, tangibly embodying a program of instructions executable by machine to perform method steps a method for verifying an integrated circuit design, said method steps comprising:

generating a model of said integrated circuit design, said integrated circuit design including simulated I/O cores, a simulated external memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus; **(Evans. Figures 2, 5, and 6. Column 2, Lines 13-37, specifically 30-32 which states, "Alternatively, the debug package could be used without the hardware components. This will, of course, not find problems that occur in the interaction of the software and the hardware. The early use of such a debug package would be tremendously beneficial to software developers in their efforts to debug software prior to the time when an entire system has been constructed. " Column 3, Lines 49-62, specifically "Virtual Components" which are loadable files and therefore software.)**

generating an external memory model, a simulated external memory mapped test device and one or more I/O driver models, said simulated external memory mapped test device including a simulated switch programmably connectable to said one or more I/O driver models, to said simulated I/O controller and to said external memory model, said I/O driver models connected to corresponding said simulated I/O cores by corresponding simulated I/O buses; **(Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus line and has a control block controlling the switchable communicative circuitry.") (Evans. Figure 5, element 146. Column 11, Line 14 which states "virtual buses.")**

loading a test case comprising a list of computer-executable instructions on said simulated processor, said loading of said test case allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said simulated external memory mapped test device to said simulated I/O controller and to said one or more of said simulated I/O cores; **(Evans. Figure 2, Element 114) (Evans. Column 2, Lines 4-6 which states "Unfortunately, software verification requires an order of magnitude more simulation patterns to verify than does hardware verification.")** and

executing test stimuli of said test case on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case. **(Evans. Figure 2, Element 114) (Evans. Column 2, Lines 4-6 which states "Unfortunately, software verification requires an order of magnitude more simulation patterns to verify than does hardware verification.")**

Evans does not explicitly disclose that every component is a simulated component representing the I/O controller, I/O cores, EMMTD, switch, I/O driver models, and bus.

However Evans teaches that software verification is an order of magnitude slower than hardware verification, therefore, the process of verification is improved by implementing certain components in hardware. This not only teaches the use of software verification for components and packages but also that the implementation discussed in **Evans** is a step forward in the art by increasing the speed and therefore decreasing the time of verification. The implementation discussed in Evans reads on the implementation discussed in the claims of the instant application. **(Evans. Column 1, Lines 31-39 for example)**

It would have been obvious to one of ordinary skill in the art to implement the verification in **Evans** by utilizing software instead of hardware in order to debug

software prior to construction of the system being verified. **(Evans. Column 2, Lines 30-32)**

Regarding Claim 33:

Evans discloses The method of claim 14, further including:

distributing said simulated external memory mapped test device and said simulated switch among a plurality of simulated external memory mapped test device modules, each simulated external memory mapped test device module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to one of said plurality of simulated external memory mapped test device modules I/O driver models: **(Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus line and has a control block controlling the switchable communicative circuitry.")** and

providing an additional simulated external memory mapped test device module directly connected to one or more additional plurality of simulated external memory mapped test device modules I/O driver models, each additional plurality of simulated external memory mapped test device modules I/O driver model of said additional plurality of simulated external memory mapped test device modules directly connected to an additional simulated I/O core, each additional simulated I/O core part of said integrated circuit design. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.) (Evans. Abstract, which states "Each bus wrapper also has switchable communicative circuitry that switchably communicatively connects each hardware model input/output pin to a bus**

line and has a control block controlling the switchable communicative circuitry.") (Evans. Figure 5, element 146. Column 11, Line 14 which states "virtual buses.")

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 34:

Evans discloses The method of claim 14, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to respective I/O driver models. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.)**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 35:

Evans discloses The method of claim 14, wherein said simulated external memory mapped test device further includes a simulated address register. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.)**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Regarding Claim 36:

Evans discloses The method of claim 14, wherein each said simulated external memory mapped test device module further includes a simulated address register. **(Evans. Column 12, Lines 31-37 which states "Each bus wrapper is individualized to accommodate the different configurations of input, output and input-output pins, distributed among various target system buses, through the inclusion of a number of registers which are loaded by the host workstation after the FPGAs are loaded with the FPGA loadable files.)**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

9. **Claim(s) 21 is** rejected under 35 U.S.C. 103(a) as being unpatentable over **Evans** in view of **Dutta et al. "Viper",** hereafter referred to as **Dutta .**

Regarding Claim 21:

Evans discloses The computer system of claim 31, wherein said one or more simulated I/O cores includes a simulated universal asynchronous receiver transmitter core, a simulated serial cores, a simulated general purpose I/O core, a direct memory access core or combinations thereof. **(Evans. Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Evans does not explicitly disclose that every component is a simulated component, see motivation statement and explanation provided in independent claims 14, 31, and 32.

Evans does not explicitly disclose The computer system of claim 31, wherein said one or more simulated I/O cores includes a simulated 1394 I/O cores.

Dutta discloses The computer system of claim 31, wherein said one or more simulated I/O cores includes a simulated 1394 I/O cores. **(Dutta. Page 21, Paragraph 3. Page 22. Figure 1)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the 1394 I/O core discussed in **Dutta** for the simulation system of **Evans** in order to allow for proper verification of all popular input output formats.

Further, the cores discussed are an intended use of claim 21. As per MPEP Section 2106, Section II.C, *"Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation."* The limitations of claim 21 are merely a type of core being verified by the system described in claim 31 and do not reflect a further limitation in the structure and therefore the scope of the claim.

Conclusion

10. All Claims are rejected.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

February 17, 2007

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100